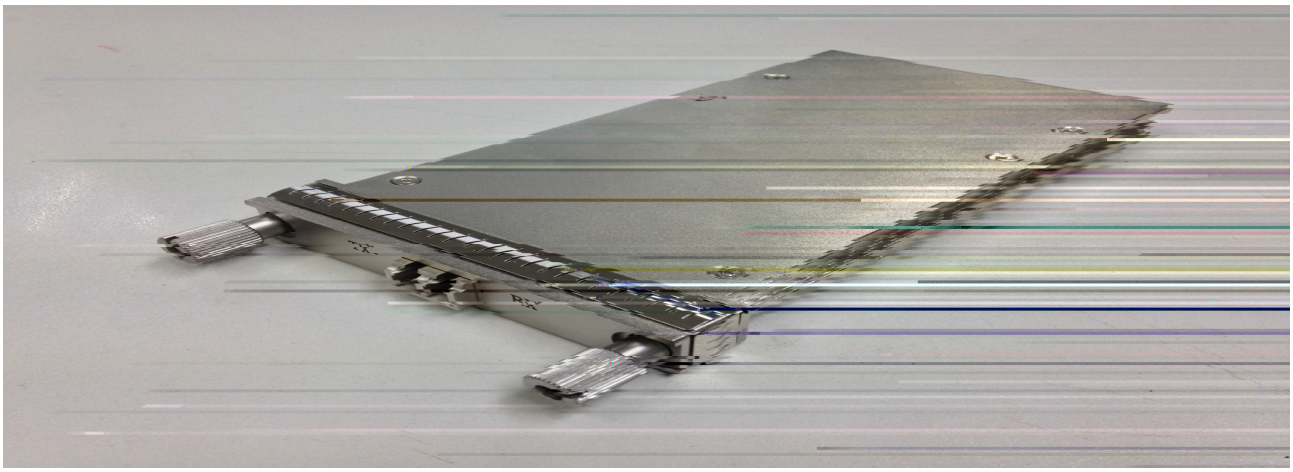
# 100Gb/s CFP Optical Transceiver

# *RTXM290-404*



## Features

- *Direct LC receptacle optical interface*
- *Single +3.3V power supply*
- *Hot-pluggable*
- *Operating optical data rate up to 112Gbps*
- *Operating electrical serial data rate up to 10.3125Gbps*
- *10 parallel electrical serial interface*
- *Transmission distance up to 10km*
- *AC coupling of CML signals*
- *1310 nm window cooled EA-DFB LD*
- *PIN ROSA*
- *Low power dissipation(Max:16W)*
- *Built in digital diagnostic function*
- *Operating case temperature range:0℃ to 70℃*
- *Compliant with RoHs*
- *MDIO Communication Interface*

## Application

- *OTN-OTU4*
- *Switch to switch interface*
- *Switch to rounter interface*
- *P to P Acess Network*

# Standards

- *Compliant with IEEE 802.3ba*
- *Compliant with CFP MSA hardware specification*
- *Compliant with CFP MSA management specification*
- *Compliant with ITU-T G.709/Y.1331*
- *Compliant with RoHS&WEEE*

# Absolute Maximum Ratings

| Parameter | Symbol | Unit | Min | Max |
|---|---|---|---|---|
| Storage Temperature Range | Ts | $^{o}$C | -40 | +85 |
| Relative Humidity | RH | % | 5 | 85 |
| Power Supply Voltage | Vcc | V | -0.5 | +3.6 |
| Operating Case Temperature Range | Tc | $^{o}$C | -5 | 75 |
| Receiver Damage Threshold Per Lane | $P_{dag}$ | dBm | +5.5 | |

# Recommended Operating Conditions

| Parameter | Symbol | Unit | Min | Typ | Max |
|---|---|---|---|---|---|
| Operating Case Temperature Range | Tc | $^{o}$C | 0 | | 70 |
| Power Supply Voltage | Vcc | V | 3.2 | 3.3 | 3.4 |
| Data rate | | Gb/s | | 103.125 | 112 |

# Specifications *(tested under recommended operating conditions, unless otherwise noted)*

| Parameter | | Symbol | Unit | Min | Typ | Max | Notes |
|---|---|---|---|---|---|---|---|
| Voltage Supply Electrical Characteristics | | | | | | | |
| Supply Current | Tx Section<br>Rx Section | Icc | A | - | - | 5 | 1 |
| Power Supply Noise | | Vrip | | | | 2%<br>3% | DC-1MHz<br>1-10MHz |
| Dissipation | Class2 | Pw | W | | | 16 | |

**Note1.** The supply current includes CFP module's supply current and test board working current.
**Note2.** Average launch power ,each lane(min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
**Note3.** Even if the TDP<1dB, the OMA(min) must exceed this value
**Note4.** Transmitter reflectance is defined looking into the transmitter
**Note5.** The receiver shall be able to tolerate , without damage, continuous exposure to an optical input signal having this average power level
**Note6.** The average receive power , each lane (max) for 100GBASE-ER4 is larger than the 100BASE-ER4 transmitter value to allow compatibility with 100BASE-LR4 units at short distances
**Note7.** Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
**Note8.** Receiver sensitivity (OMA), each lane (max) is informative
**Note9.** Measured with PRBS $2^{31}$-1 for BER=$10^{-5}$. The BER for the OTU4 application is required to be met only after FEC has been applied.
**Note10.** Measured with conformance test signal at TP3 for BER=$10^{-12}$
**Note11.** conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB;stressed eye J2 jitter for each lane is 0.3UI; stressed eye J9 jitter for each lane is 0.47UI.

# Hardware Control Pins

The CFP Module support real-time control functions via hardware pins, listed in the following table: Hardware Control Pins

Hardware Control Pins

| Pin # | Symbol | Description | I/O | Logic | H | L | Pull-up/down |
|---|---|---|---|---|---|---|---|
| 30 | PRG_CNTL1 | Programmable Control 1 MSADefault:TRXIC_RSTn , TX&RX ICs reset, "0":reset;"1" | I | 3.3V LVCMOS | per CFP MSA Management Interface Specification | | Pull-Up Note1 |
| 31 | PRG_CNTL2 | Programmable Control 2 MSADefault :Hardware Interlock LSB | I | 3.3V LVCMOS | | | Pull-Up Note1 |
| 32 | PRG_CNTL3 | Programmable Control 3 MSA Default:Hardware Interlock MSB | I | 3.3V LVCMOS | | | Pull-Up Note1 |
| 36 | TX_DIS | Transmitter Disable | I | 3.3V LVCMOS | Disable | Enable | Pull-Up Note1 |
| 37 | MOD_LOPWR | Module Low Power Mode | I | 3.3V LVCMOS | Low Power | Enable | Pull-Up Note1 |
| 39 | MOD_RSTn | Module Reset(Invert) | I | 3.3V LVCMOS | Enable | Reset | Pull-Down Note2 |

**Note1:** Pull-Up resistor (4.7KOhm to 10 KOhm) is located within the CFP module
**Note2:** Pull-Down resistor (4.7KOhm to 10 kOhm) is located within the CFP module

# Hardware Alarm Pins

The CFP Module supports alarm hardware pins listed in the following table: Hardware Alarm Pins

Hardware Alarm Pins

| Pin # | Symbol | Description | I/O | Logic | H | L | Pull-up/down |
|---|---|---|---|---|---|---|---|
| 33 | PRG_ALRM1 | Programmable Alarm 1 MSA | O | 3.3V LVCMOS | Active High per MDIO document | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | Default:HIPWR_ON | | | | |
| 34 | PRG_ALRM 2 | Programmable Alarm 2 MSA default:MOD_READY, Ready State has been reached | O | 3.3V LVCMOS | | |
| 35 | PRG_ALRM 3 | Programmable Alarm 3 MSA Default: MOD_FAULT | O | 3.3V LVCMOS | | |

| | | | | | |
|---|---|---|---|---|---|
| | | | | | Vendor Datasheet |
| Hardware MOD_LOPWR deassert | t_MOD_LOPWR_deassert | | | ms | Value is dependent upon module start-up time.Please See register"Maximum High-Power-up ime"in "CFP MSA Management Interface Specification" |
| Receiver Loss of Signal Assert Time | t_loss_assert | | 100 | us | Maximum value designed to support telecom applications |
| Receiver Loss of Signal De-Assert Time | t_loss_deassert | | 100 | us | Maximum value designed to support telecom applications |
| Global Alarm Assert Delay Time | GLB_ALRMn_assert | | 150 | ms | This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details |
| Global Alarm De-assert Delay Time | GLB_ALRMn_deassert | | 150 | ms | This is a logical "OR" of Associated MDIO alarm& status registers.Please see MDIO document for further details |
| Management Interface Clock Period | t_prd | 250 | | ns | MDC is 4MHz rate |
| Host MDIO t_setup | t_setup | 10 | | ns | |
| Host MDIO t_hold | t_hold | 10 | | ns | |
| CFP MDIO t_delay | t_delay | 0 | 175 | ns | |
| Initialization time from Reset | t_initialize | | 2.5 | s | |
| Transmitter Disabled(TX_DIS_asserted) | t_deassert | | 100 | us | Application Specific |
| Transmitter Enabled(TX_DIS_asserted) | t_assert | | 10 | ms | Value is dependent upon module start-up time.Please See register "Maximum TX-Turn-on Time" in "CFP MSA Management Interface Specification" |

# High Speed Electrical Characteristics

Reference Clock Characteristics

| | | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Impedance | Zd | 80 | 100 | 120 | Ω | |
| Frequency | | | 161.1328125/644.53125 | | MHz | 1/64 or 1/16 of electrical lane rate |
| Frequency Stability | △f | -100 | | 100 | ppm | For Ethernet applications |
| | | -20 | | 20 | | For Telecom applications |
| Output Differential Voltage | $V_{DIFF}$ | 400 | | 1200 | mV | Peak to Peak Differential |
| RMS jitter[1,2] | σ | | | 10 | ps | Random Jitter Over frequency band of 10KHz<f<10MHz |
| Clock Duty Cycle | | 40 | | 60 | % | |
| Clock Rise/Fall Time 10%/90% | $t_{r/f}$ | 200 | | 1250 | ps | 1/64 of electrical lane rate |
| | | 50 | | 315 | | 1/16 of electrical lane rate |

Note1: The term “40GBASE_FR” is the 40GbE serial optical interface in the task force phase at IEEE-SA at the time of this publication. Also, 1/16 of optical lane clock is recommended for TX_MCLK and RX_MCLK

Note2: Multi-protocol modules are recommended to adopt the clock rate rate used in Telecom applications

Optional Transmitter and Receiver Monitor Clock Characteristics

| | | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Impedance | Zd | 80 | 100 | 120 | Ω | |
| Frequency | | | | | MHz | 1/8 of Network lane rate |
| Output Differential Voltage | $V_{DIFF}$ | 400 | | 1200 | mV | Peak to Peak Differential |
| Clock Duty Cycle | | 40 | | 60 | % | |

# CFP Register Allocation

CFP Register Allocation

| Staring Address in Hex | Ending Address in Hex | Access Type | Allocated Size | Data Bit Width | Table Name and Description |
|---|---|---|---|---|---|
| 0000 | 7FFF | N/A | 32768 | N/A | Reserved for IEEE 802.3 use |
| 8000 | 807F | RO | 128 | 8 | CFP NVR 1.Basic ID register |
| 8080 | 80FF | RO | 128 | 8 | CFP NVR 2.Extended ID register |
| 8100 | 817F | RO | 128 | 8 | CFP NVR 3. Network lane specific registers |
| 8180 | 81FF | RO | 128 | 8 | CFP NVR 4 |
| 8200 | 83FF | RO | 4x128 | N/A | MSA Reserved |
| 8400 | 847F | RO | 128 | 8 | Vendor NVR 1. Vendor data registers |
| 8480 | 84FF | RO | 128 | 8 | Vendor NVR 2. Vendor data registers |
| 8500 | 87FF | RO | 6x128 | N/A | Reserved by CFP MSA |
| 8800 | 887F | R/W | 128 | 8 | User NVR 1. User data registers |
| 8880 | 88FF | R/W | 128 | 8 | User NVR 2. User data registers |

| | | | | | |
|---|---|---|---|---|---|
| 8900 | 8EFF | RO | 12x128 | N/A | Reserved by CFP MSA |
| 8F00 | 8FFF | N/A | 2x128 | N/A | Reserved for User private use |
| 9000 | 9FFF | RO | 4096 | N/A | Reserved for vendor private use |
| A000 | A07F | R/W | 128 | 16 | CFP Module VR1. CFP Module level control and DDM registers |
| A080 | A0FF | RO | 128 | 16 | Reserved by CFP MSA |
| A100 | A1FF | RO | 2x128 | N/A | Reserved by CFP MSA |
| A200 | A27F | R/W | 128 | 16 | etwork Lane VR 1.Network lane specific register |
| A280 | A2FF | R/W | 128 | 16 | Network Lane VR 2.Network lane specific register |
| A300 | A3FF | RO | 2x128 | N/A | Reserved by CFP MSA |
| A400 | A47F | R/W | 128 | 16 | Host lane VR1. Host lane specific registers |
| A480 | AFFF | RO | 23x128 | N/A | Reserved by CFP MSA |
| B000 | FFFF | RO | 5x4096 | N/A | Reserved by CFP MSA |

# CFP NVR1

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | Power per Connector | | |
| 801C | 1 | RO | 7~0 | Maximum Optical Input Power per Network Lane | | |
| 801D | 1 | RO | 7~0 | Maximum Power Consumption | | |
| 801E | 1 | RO | 7~0 | Maximum Power Consumption in Low Power Mode | | |
| 801F | 1 | RO | 7~0 | Maximum Operating Case Temp Range | | |
| 8020 | 1 | RO | 7~0 | Minimum Operating Case Temp Range | | |
| 8021 | 16 | RO | 7~0 | Vendor Name | | |
| 8031 | 3 | RO | 7~0 | Vendor OUI | | |
| 8034 | 16 | RO | 7~0 | Vendor Part Number | | |
| 8044 | 16 | RO | 7~0 | Vendor Serial Number | | |
| 8054 | 8 | RO | 7~0 | Data Code | | |
| 805C | 2 | RO | 7~0 | Lot Code | | |
| 805E | 10 | RO | 7~0 | CLEI Code | | |
| 8068 | 1 | RO | 7~0 | CFP MSA hardware Specification Revision Number | | |
| 8069 | 1 | RO | 7~0 | CFP MSA Management Interface Specification Revision Number | | |
| 806A | 2 | RO | 7~0 | Module Hardware Version Number | | |
| 806C | 2 | RO | 7~0 | Module Firmware Version Number | | |
| 806E | 1 | RO | 7~0 | Digital Diagnostic Monitoring Type | | |
| 806F | 1 | RO | 7~0 | Digital Diagnostic Monitoring Capability 1 | | |
| 8070 | 1 | RO | 7~0 | Digital Diagnostic Monitoring Capability 2 | | |
| 8071 | 1 | RO | 7~0 | Module Enhanced Options | | |
| 8072 | 1 | RO | 7~0 | Maximum High-Power-up Time | | |
| 8073 | 1 | RO | 7~0 | Maximum TX-Turn-on Time | | |
| 8074 | 1 | RO | 7~0 | Host Lane Signal Spec | | |
| 8075 | 1 | RO | 7~0 | Heat Sink Type | | |
| 8076 | 1 | RO | 7~0 | Maximum TX-Turn-off Time | | |
| 8077 | 1 | RO | 7~0 | Maximum High-Power-down Time | | |
| 8078 | 1 | RO | 7~0 | Module Enhanced Options 2 | | |
| 8079 | 1 | RO | 7~0 | Transmitter Monitor Clock Options | | |
| 807A | 1 | RO | 7~0 | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 808C | 2 | RO | 7~0 | VCC Low Warning Threshold | | |
| 808E | 2 | RO | 7~0 | VCC Low Alarm Threshold | | |
| 8090 | 2 | RO | 7~0 | SOA Bias Current High Alarm Threshold | | |
| 8092 | 2 | RO | 7~0 | SOA Bias Current High Warning Threshold | | |
| 8094 | 2 | RO | 7~0 | SOA Bias Current Low Warning Threshold | | |
| 8096 | 2 | RO | 7~0 | SOA Bias Current Low Alarm Threshold | | |
| 8098 | 2 | RO | 7~0 | Auxili05 059Cs1 cs 0 0 0 sc q0.2 | | |

# CFP NVR3

**Network Lane BOL Measurement Registers**

| Hex Addr | Size | Access Type | Bit | Register Name | Content (HEX) | LSB Unit |
|---|---|---|---|---|---|---|
| Base ID Information | | | | | | |
| 8100 | 32 | RO | 7~0 | Rx Sensitivity Spec for network lanes 0~15 | | |
| 8120 | 32 | RO | 7~0 | Tx Power Spec for network lanes 0~15 | | |
| 8140 | 32 | RO | 7~0 | Measured ER for network lanes 0~15 | | |
| 8160 | 32 | RO | 7~0 | Path Penalty for network lanes 0~15 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | RW | 7~0 | Alarm Source Code | | |
| A00B | 1 | RO | | Module Bi-/Uni-Directional Operating Mode Select | | |
| | | | 15~3 | Reserved | | |
| | | RW | 2~0 | Module Bi/uni-Direction Mode Select | | |
| A00C | 4 | RO | | Reserved | | |
| Module Control Registers | | | | | | |
| A010 | 1 | | | **Module General Control** | | |
| | | RW/SC/LH | 15 | Soft Module Reset | | |
| | | RW | 14 | Soft Module Low Power | | |
| | | RW | 13 | Soft TX Disable | | |
| | | RW | 12 | Soft PRG_CNTL3 Control | | |
| | | RW | 11 | Soft PRG_CNTL2 Control | | |
| | | RW | 10 | Soft PRG_CNTL1 Control | | |
| | | RW | 9 | Soft GLB_ALRM Test | | |
| | | RO | 8~6 | Reserved | | |
| | | RO | 5 | TX_DIS Pin State | | |
| | | RO | 4 | MOD_LOPWR Pin State | | |
| | | RO | 3 | PRG_CNTL3 Pin State | | |
| | | RO | 2 | PRG_CNTL2 Pin State | | |
| | | RO | 1 | PRG_CNTL1 Pin State | | |
| | | RO | 0 | Reserved | | |
| A011 | 1 | | | **Netwowk Lane TX Control** | | |
| | | RO | 15 | Reserved | | |
| | | RW | 14 | TX PRBS Generator Enable | | |
| | | RW | 13 | TX PRBS Pattern 1 | | |
| | | RW | 12 | TX PRBS Pattern 0 | | |
| | | RW | 11 | TX De-skew Enable | | |
| | | RW | 10 | TX FIFO Reset | | |
| | | RW | 9 | TX FIFO Auto Reset | | |
| | | RW | 8 | TX Reset | | |
| | | RW | 7~5 | TX MCLK Control | | |
| | | RO | 4 | Reserved | | |
| | | RW | 3~1 | TX Rate Select (10G lane rate) | | |
| | | RW | 0 | TX Reference CLK Rate Select | | |
| A012 | 1 | | | **Network Lane RXControl** | | |
| | | RW | 15 | Active Decision Voltageand Phase function | | |
| | | RW | 14 | RX PRBS CheckerEnable | | |
| | | RW | 13 | RX PRBS Pattern 1 | | |
| | | RW | 12 | RX PRBS Pattern 0 | | |
| | | RW | 11 | RX Lock RX_MCLK to Reference CLK | | |
| | | RW | 10 | Network Lane Loop-back | | |
| | | RW | 9 | RX FIFO Auto Reset | | |
| | | RW | 8 | RX Reset | | |
| | | RW | 7~5 | RX MCLK Control | | |
| | | RW | 4 | RX FIFO Reset | | |
| | | RW | 3~1 | RX Rate Select | | |
| | | RW | 0 | RX Reference CLK Rate Select | | |
| A013 | 1 | RW | | **Individual Network Lane TX_DIS Control** | | |
| | | | 15 | Lane 15 Disable | | |
| | | | 14 | Lane 14 Disable | | |
| | | | 13 | Lane 13 Disable | | |
| | | | 12 | Lane 12 Disable | | |
| | | | 11 | Lane 11 Disable | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | 10 | Lane 10 Disable | | |
| | | | 9 | Lane 9 Disable | | |
| | | | 8 | Lane 8 Disable | | |
| | | | 7 | Lane 7 Disable | | |
| | | | 6 | Lane 6 Disable | | |
| | | | 5 | Lane 5 Disable | | |
| | | | 4 | Lane 4 Disable | | |
| | | | 3 | Lane 3 Disable | | |
| | | | 2 | Lane 2 Disable | | |
| | | | 1 | Lane 1 Disable | | |
| | | | 0 | Lane 0 Disable | | |
| A014 | 1 | | | **Host Lane Control** | | |
| | | RO | 15 | Reserved | | |
| | | RW | 14 | TX PRBS Checker Enable | | |
| | | RW | 13 | TX PRBS Pattern 1 | | |
| | | RW | 12 | TX PRBS Pattern 0 | | |
| | | RO | 11 | Reserved | | |
| | | RW | 10 | Host Lane Loop-back Enable | | |
| | | RO | 9 | Reserved | | |
| | | RO | 8 | Reserved | | |
| | | RW | 7 | RX PRBS Generator Enable | | |
| | | RW | 6 | RX PRBS Pattern 1 | | |
| | | RW | 5 | RX PRBS Pattern 0 | | |
| | | RO | 4~0 | Reserved | | |
| A015 | 1 | RO | | Reserved | | |
| A016 | 1 | RO | | **Module State** | | |
| | | | 15~9 | Reserved | | |
| | | | 8 | High-Power-down State | | |
| | | | 7 | TX-Turn-off State | | |
| | | | 6 | Fault State | | |
| | | | 5 | Ready State | | |
| | | | 4 | TX-Turn-on State | | |
| | | | 3 | TX-Off State | | |
| | | | 2 | High-Power-up State | | |
| | | | 1 | Low-Power State | | |
| | | | 0 | Initialize State | | |
| A017 | 1 | RO | | Reserved | | |
| A018 | 1 | RO | | **Global Alarm Summary** | | |
| | | | 15 | GLB_ALRM Assertion Status | | |
| | | | 14 | Host Lane Fault and Status Summary | | |
| | | | 13 | Network Lane Fault and Status Summary | | |
| | | | 12 | Network Lane Alarm and Warning Summary | | |
| | | | 11 | Module Alarm and Warning 2 Summary | | |
| | | | 10 | Module Alarm and Warning 1 Summary | | |
| | | | 9 | Module Fault Summary | | |
| | | | 8 | Module General Status Summary | | |
| | | | 7 | Module State Summary | | |
| | | | 6~1 | Reserved | | |
| | | | 0 | Soft GLB_ALRM Test Status | | |
| A019 | 1 | RO | | **Network Lane Alarm and Warning Summary** | | |
| | | | 15 | Lane 15 Alarm and Warning Summary | | |
| | | | 14 | Lane 14 Alarm and Warning Summary | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | 13 | Lane 13 Alarm and Warning Summary | | |
| | | | 12 | Lane 12 Alarm and Warning Summary | | |
| | | | 11 | Lane 11 Alarm and Warning Summary | | |
| | | | 10 | Lane 10 Alarm and Warning Summary | | |
| | | | 9 | Lane 9 Alarm and Warning Summary | | |
| | | | 8 | Lane 8 Alarm and Warning Summary | | |
| | | | 7 | Lane 7 Alarm and Warning Summary | | |
| | | | 6 | Lane 6 Alarm and Warning Summary | | |
| | | | 5 | Lane 5 Alarm and Warning Summary | | |
| | | | 4 | Lane 4 Alarm and Warning Summary | | |
| | | | 3 | Lane 3 Alarm and Warning Summary | | |
| | | | 2 | Lane 2 Alarm and Warning Summary | | |
| | | | 1 | Lane 1 Alarm and Warning Summary | | |
| | | | 0 | Lane 0 Alarm and Warning Summary | | |
| A01A | 1 | RO | | **Network Lane Fault and Status Summary** | | |
| | | | 15 | Lane 15 Fault and Status Summary | | |
| | | | 14 | Lane 14 Fault and Status Summary | | |
| | | | 13 | Lane 13 Fault and Status Summary | | |
| | | | 12 | Lane 12 Fault and Status Summary | | |
| | | | 11 | Lane 11 Fault and Status Summ Tm /TW n /Cs10 37 0 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| A01B | 1 | RO | | **Host Lane Fault and Status Summary** | | |
| | | | 15 | Lane 15 Fault and Status Summary | | |
| | | | 14 | Lane 14 Fault and Status Summary | | |
| | | | 13 | Lane 13 Fault and Status Summary | | |
| | | | 12 | Lane 12 Fault and Status Summary | | |
| | | | 11 | Lane 11 Fault and Status Summary | | |
| | | | 10 | Lane 10 Fault and Status Summary | | |
| | | | 9 | Lane 9 Fault and Status Summary | | |
| | | | 8 | Lane 8 Fault and Status Summary | | |
| | | | 7 | Lane 7 Fault and Status Summary | | |
| | | | 6 | Lane 6 Fault and Status Summary | | |
| | | | 5 | Lane 5 Fault and Status Summary | | |
| | | | 4 | Lane 4 Fault and Status Summary | | |
| | | | 3 | Lane 3 Fault and Status Summary | | |
| | | | 2 | Lane 2 Fault and Status Summary | | |
| | | | 1 | Lane 1 Fault and Status Summary | | |
| | | | 0 | Lane 0 Fault and Status Summary | | |
| A01C | 1 | RO | | Reserved | | |
| Module FAWS Registers | | | | | | |
| A01D | 1 | RO | | **Module General Status** | | |
| | | | 15 | Reserved | | |
| | | | 14 | Reserved | | |
| | | | 13 | HW_Interlock | | |
| | | | 12~11 | Reserved | | |
| | | | 10 | Loss of REFCLK Input | | |
| | | | 9 | TX_JITTER_PLL_LOL | | |
| | | | 8 | TX_CMU_LOL | | |
| | | | 7 | TX_LOSF | | |
| | | | 6 | TX_HOST_LOL | | |
| | | | 5 | RX_LOS | | |
| | | | 4 | RX_NETWORK_LOL | | |
| | | | 3 | Out of Alignment | | |
| | | | 2 | Reserved | | |
| | | | 1 | HIPWR_ON | | |
| | | | 0 | Reserved | | |
| A01E | 1 | RO | | **Module Fault Status** | | |
| | | | 15 | Reserved | | |
| | | | 14~7 | Reserved | | |
| | | | 6 | PLD or Flash Initialization Fault | | |
| | | | 5 | Power Supply Fault | | |
| | | | 4~2 | Reserved | | |
| | | | 1 | CFP Checksum Fault | | |
| | | | 0 | Reserved | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| A01F | 1 | RO | | **Module Alarms and Warnings 1** | | |
| | | | 15~12 | Reserved | | |
| | | | 11 | Mod Temp High Alarm | | |
| | | | 10 | Mod Temp High Warning | | |
| | | | 9 | Mod Temp Low Warning | | |
| | | | 8 | Mod Temp Low Alarm | | |
| | | | 7 | Mod Vcc High Alarm | | |
| | | | 6 | Mod Vcc High Warning | | |
| | | | 5 | Mod Vcc Low Warning | | |
| | | | 4 | Mod Vcc Low Alarm | | |
| | | | 3 | Mod SOA Bias High Alarm | | |
| | | | 2 | Mod SOA Bias High Warning | | |
| | | | 1 | Mod SOA Bias Low Warning | | |
| | | | 0 | Mod SOA Bias Low Alarm | | |
| A020 | 1 | RO | | **Module Alarms and Warnings 2** | | |
| | | | 15~8 | Reserved | | |
| | | | 7 | Mod Aux 1 High Alarm | | |
| | | | 6 | Mod Aux 1 High Warning | | |
| | | | 5 | Mod Aux 1 Low Warning | | |
| | | | 4 | Mod Aux 1 Low Alarm | | |
| | | | 3 | Mod Aux 2 High Alarm | | |
| | | | 2 | Mod Aux 2 High Warning | | |
| | | | 1 | Mod Aux 2 Low Warning | | |
| | | | 0 | Mod Aux 2 Low Alarm | | |
| A021 | 1 | RO | | Reserved | | |
| A022 | 1 | | | **Module State Latch** | | |
| | | RO | 15~9 | Reserved | | |
| | | RO/LH/COR | 8 | High-Power-down State Latch | | |
| | | RO/LH/COR | 7 | TX-Turn-off State Latch | | |
| | | RO/LH/COR | 6 | Fault State Latch | | |
| | | RO/LH/COR | 5 | Ready State Latch | | |
| | | RO/LH/COR | 4 | TX-Turn-on State Latch | | |
| | | RO/LH/COR | 3 | TX-Off State Latch | | |
| | | RO/LH/COR | 2 | High-Power-up State Latch | | |
| | | RO/LH/COR | 1 | Low-Power State Latch | | |
| | | RO/LH/COR | 0 | Initialize State Latch | | |
| A023 | 1 | | | **Module General Status Latch** | | |
| | | RO | 15 | Reserved | | |
| | | RO | 14 | Reserved | | |
| | | RO/LH/COR | 13 | HW_Interlock Latch | | |
| | | RO | 12~11 | Reserved | | |
| | | RO/LH/COR<br>RO/LH/COR | 10 | Loss of REFCLK Input Latch | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | RO | 0 | Reserved | | |
| A025 | 1 | | | **Module Alarms and Warnings 1 Latch** | | |
| | | RO | 15~12 | Reserved | | |
| | | RO/LH/COR | 11 | Mod Temp High Alarm Latch | | |
| | | RO/LH/COR | 10 | Mod Temp High Warning Latch | | |
| | | RO/LH/COR | 9 | Mod Temp Low Warning Latch | | |
| | | RO/LH/COR | 8 | Mod Temp Low Alarm Latch | | |
| | | RO/LH/COR | 7 | Mod Vcc High Alarm Latch | | |
| | | RO/LH/COR | 6 | Mod Vcc High Warning Latch | | |
| | | RO/LH/COR | 5 | Mod Vcc Low Warning Latch | | |
| | | RO/LH/COR | 4 | Mod Vcc Low Alarm Latch | | |
| | | RO/LH/COR | 3 | Mod SOA Bias High Alarm Latch | | |
| | | RO/LH/COR | 2 | Mod SOA Bias High Warning Latch | | |
| | | RO/LH/COR | 1 | Mod SOA Bias Low Warning Latch | | |
| | | RO/LH/COR | 0 | Mod SOA Bias Low Alarm Latch | | |
| A026 | 1 | | | **Module Alarms and Warnings 2 latch** | | |
| | | RO | 15~8 | Reserved | | |
| | | RO/LH/COR | 7 | Mod Aux 1 High Alarm Latch | | |
| | | RO/LH/COR | 6 | Mod Aux 1 High Warning Latch | | |
| | | RO/LH/COR | 5 | Mod Aux 1 Low Warning Latch | | |
| | | RO/LH/COR | 4 | Mod Aux 1 Low Alarm Latch | | |
| | | RO/LH/COR | 3 | Mod Aux 2 High Alarm Latch | | |
| | | RO/LH/COR | 2 | Mod Aux 2 High Warning Latch | | |
| | | RO/LH/COR | 1 | Mod Aux 2 Low Warning Latch | | |
| | | RO/LH/COR | 0 | Mod Aux 2 Low Alarm Latch | | |
| A027 | 1 | RO | | Reserved | | |
| A028 | 1 | | | **Module Stable Enable** | | |
| | | RO | 15~9 | Reserved | | |
| | | RW | 8 | High-Power-down State Enable | | |
| | | RW | 7 | TX-Turn-off State Enable | | |
| | | RW | 6 | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | RW | 5 | RX_LOS Enable | | |
| | | RW | 4 | RX_NETWORK_LOL Enable | | |
| | | RW | 3 | Out of Alignment Enable | | |
| | | RO | 2~0 | Reserved | | |
| A02A | 1 | | | **Module Fault Status Enable** | | |
| | | RO | 15~7 | Reserved | | |
| | | RW | 6 | PLD or Flash Initialization Fault Enable | | |
| | | RW | 5 | Power Supply Fault Enable | | |
| | | RO | 4~2 | Reserved | | |
| | | RW | 1 | CFP Checksum Fault Enable | | |
| | | RO | 0 | Reserved | | |
| A02B | 1 | RO | | Module Alarm and Warnings 1 Enable | | |
| | | | 15~12 | Reserved | | |
| | | | 11 | Mod Temp Hi Alarm Enable | | |
| | | | 10 | Mod Temp Hi Warn Enable | | |
| | | | 9 | Mod Temp Low Warning Enable | | |
| | | | 8 | Mod Temp Low Alarm Enable | | |
| | | | 7 | Mod Vcc High Alarm Enable | | |
| | | | 6 | Mod Vcc High Warning Enable | | |
| | | | 5 | Mod Vcc Low Warning Enable | | |
| | | | 4 | Mod Vcc Low Alarm Enable | | |
| | | | 3 | Mod SOA Bias High Alarm Enable | | |
| | | | 2 | Mod SOA Bias High Warning Enable | | |
| | | | 1 | Mod SOA Bias Low Warning Enable | | |
| | | | 0 | Mod SOA Bias Low Alarm Enable | | |
| A02C | 1 | | | **Module Alarms and Warnings Enable** | | |
| | | RO | 15~8 | Reserved | | |
| | | RW | 7 | Mod Aux 1 High Alarm Enable | | |
| | | | 6 | Mod Aux 1 High Warning Enable | | |
| | | | 5 | Mod Aux 1 Low Warning Enable | | |
| | | | 4 | Mod Aux 1 Low Alarm Enable | | |
| | | | 3 | Mod Aux 2 High Alarm Enable | | |
| | | | 2 | Mod Aux 2 High Warning Enable | | |
| | | | 1 | Mod Aux 2 Low Warning Enable | | |
| | | | 0 | Mod Aux 2 Low Alarm Enable | | |
| A02D | 2 | RO | | Reserved | | |
| Module Analog A/D Value Registers | | | | | | |
| A02F | 1 | RO | 15~0 | Module Temp Monitor A/D Value | | |
| A030 | 1 | RO | 15~0 | Module Power supply | | |
| | | | | 3.3 V Monitor A/D Value | | |
| A031 | 1 | RO | 15~0 | SOA Bias Current A/D Value | | |
| A032 | 1 | RO | 15~0 | Module Auxiliary 1 Monitor A/D Value | | |

A033 1

| | | | | | | |
|---|---|---|---|---|---|---|
| A220 | 16 | RO/LH/COR | | **Network Lane n Alarm and Warning Latch** | | |
| | | | 15 | Bias High Alarm Latch | | |
| | | | 14 | Bias High Warning Latch | | |
| | | | 13 | Bias Low Warning Latch | | |
| | | | 12 | Bias Low Alarm Latch | | |
| | | | 11 | TX Power High Alarm Latch | | |
| | | | 10 | TX Power High Warning Latch | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | Alarm Enable | | |
| | | | 3 | RX Power High Alarm Enable | | |
| | | | 2 | RX Power High Warning Enable | | |
| | | | 1 | RX Power Low Warning Enable | | |
| | | | 0 | RX Power Low Alarm Enable | | |
| A250 | 16 | | | **Network Lane n Fault and Status Enable** | | |
| | | RW | 15 | Lane TEC Fault Enable | | |
| | | RW | 14 | Lane Wavelength Unlocked Fault Enable | | |
| | | RW | 13 | Lane APD Power Supply Fault Enable | | |
| | | RO | 12~8 | Reserved | | |
| | | RW | 7 | Lane TX_LOSF Enable | | |
| | | RW | 6 | Lane TX_LOL Enable | | |
| | | RO | 5 | Reserved | | |
| | | RW | 4 | Lane RX_LOS Enable | | |
| | | RW | 3 | Lane RX_LOL Enable | | |
| | | RW | 2 | Lane RX FIFO Status Enable | | |
| | | RO | 1~0 | Reserved | | |
| A260 | 32 | RO | | Reserved | | |

# CFP Network Lane VR2

**Network Lane VR2**

Network Lane VR1

**Host Lane VR1**

| Host Lane VR1 | | | | | | |
|---|---|---|---|---|---|---|
| Hex Addr | Size | Access Type | Bit | Register Name | Content (HEX) | LSB Unit |
| **Host Lane FAWS Status Registers** | | | | | | |
| A400 | 16 | | | | | |

| | Name | | | | Name | | |
|---|---|---|---|---|---|---|---|
| 148 | GND | 1 | 3.3V_GND | 111 | GND | 38 | MOD_ABS |
| 147 | REFCLKn | 2 | 3.3V_GND | 110 | N.C | 39 | MOD_RSTn |
| 146 | REFCLKp | 3 | 3.3V_GND | 109 | N.C | 40 | RX_LOS |
| 145 | GND | 4 | 3.3V_GND | 108 | GND | 41 | GLB_ALRMn |
| 144 | N.C. | 5 | 3.3V_GND | 107 | RX9n | 42 | PRTADR4 |
| 143 | N.C. | 6 | 3.3V | 106 | RX9p | 43 | PRTADR3 |
| 142 | GND | 7 | 3.3V | 105 | GND | 44 | PRTADR2 |
| 141 | TX9n | 8 | 3.3V | 104 | RX8n | 45 | PRTADR1 |
| 140 | TX9n | 9 | 3.3V | 103 | RX8p | 46 | PRTADR0 |
| 139 | GND | 10 | 3.3V | 102 | GND | 47 | MDIO |
| 138 | TX8n | 11 | 3.3V | 101 | RX7n | 48 | MDC |
| 137 | TX8p | 12 | 3.3V | 100 | RX7p | 49 | GND |
| 136 | GND | 13 | 3.3V | 99 | GND | 50 | VND_IO_F |
| 135 | TX7n | 14 | 3.3V | 98 | RX6n | 51 | VND_IO_G |
| 134 | TX7p | 15 | 3.3V | 97 | RX6p | 52 | GND |
| 133 | GND | 16 | 3.3V_GND | 96 | GND | 53 | VND_IO_H |
| 132 | TX6n | 17 | 3.3V_GND | 95 | RX5n | 54 | VND_IO_J |
| 131 | TX6p | 18 | 3.3V_GND | 94 | RX5p | 55 | 3.3V_GND |
| 130 | GND | 19 | 3.3V_GND | 93 | GND | 56 | 3.3V_GND |
| 129 | TX5n | 20 | 3.3V_GND | 92 | RX4n | 57 | 3.3V_GND |
| 128 | TX5p | 21 | VND_IO_A | 91 | RX4p | 58 | 3.3V_GND |
| 127 | GND | 22 | VND_IO_B | 90 | GND | 59 | 3.3V_GND |
| 126 | TX4n | 23 | GND | 89 | RX3n | 60 | 3.3V |
| 125 | TX4p | 24 | TX_MCLKn | 88 | RX3p | 61 | 3.3V |
| 124 | GND | 25 | TX_MCLKp | 87 | GND | 62 | 3.3V |
| 123 | TX3n | 26 | GND | 86 | RX2n | 63 | 3.3V |
| 122 | TX3p | 27 | VND_IO_C | 85 | RX2p | 64 | 3.3V |
| 121 | GND | 28 | VND_IO_D | 84 | GND | 65 | 3.3V |
| 120 | TX2n | 29 | VND_IO_E | 83 | RX1n | 66 | 3.3V |

| PIN# | Name | I/O | Logic | Description |
|---|---|---|---|---|
| 1 | 3.3V_GND | | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal |
| 2 | 3.3V_GND | | | |
| 3 | 3.3V_GND | | | |
| 4 | 3.3V_GND | | | |
| 5 | 3.3V_GND | | | |
| 6 | 3.3V | | | 3.3V Module Supply Votage |
| 7 | 3.3V | | | |
| 8 | 3.3V | | | |
| 9 | 3.3V | | | |
| 10 | 3.3V | | | |
| 11 | 3.3V | | | |
| 12 | 3.3V | | | |
| 13 | 3.3V | | | |
| 14 | 3.3V | | | |
| 15 | 3.3V | | | |
| 16 | 3.3V_GND | | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal |
| 17 | 3.3V_GND | | | |
| 18 | 3.3V_GND | | | |
| 19 | 3.3V_GND | | | |
| 20 | 3.3V_GND | | | |
| 21 | VND_IO_A | I/O | | Module Vendor I/O. Do Not Connect |
| 22 | VND_IO_B | I/O | | Module Vendor I/O. Do Not Connect |
| 23 | GND | | | |
| 24 | TX_MCLKn | O | CML | For optical waveform testing. Not for normal use |
| 25 | TX_MCLKp | O | CML | For optical waveform testing. Not for normal use |
| 26 | GND | | | |
| 27 | VND_IO_C | I/O | | Module Vendor I/O C. Do Not Connect |
| 28 | VND_IO_D | I/O | | Module Vendor I/O C. Do Not Connect |
| 29 | VND_IO_E | I/O | | Module Vendor I/O C. Do Not Connect |
| 30 | PRG_CNTL1 | I | LVCMOS w/PUR | Programmable Control 1 set over MDIO. MSA Default: TRXIC_RSTn, TX&RX ICs reset,"0" Reset, "1" or NC: enabled=not used |
| 31 | PRG_CNTL2 | I | LVCMOS w/PUR | Programmable Control 2 set over MDIO. MSA Default: Hardware Interlock LSB, "00"≤8W, "01" ≤16W, "10" ≤24W, "11" or NC≤24W=not used |

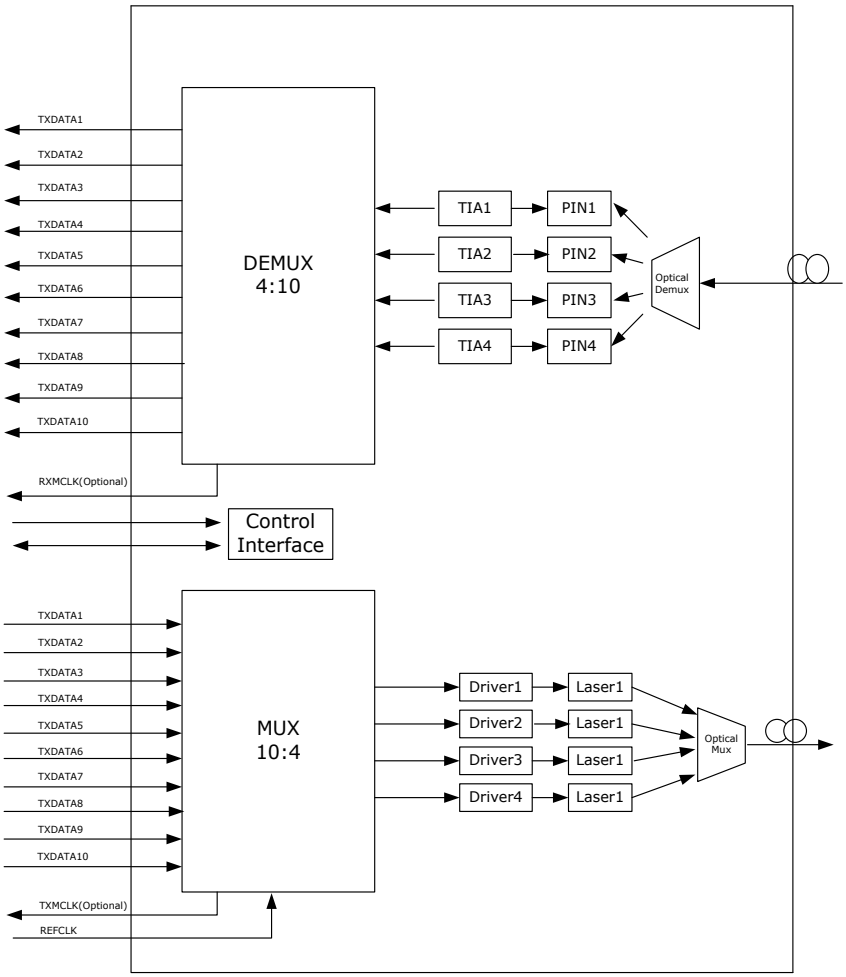
| | | | | |
|---|---|---|---|---|
| 32 | PRG_CNTL3 | I | LVCMOS w/PUR | Programmable Control 2 set over MDIO. MSA Default: Hardware Interlock MSB, “00”≤8W, “01” ≤16W, “10” ≤24W, “11” or NC≤24W=not used |
| 33 | PRG_ALRM1 | O | LVCMOS | Programmable Alarm 1 set over MDIO, MSA Default: HIPWR_ON.”1”:module power up completed,”0”: module not high powered up |
| 34 | PRG_ALRM2 | O | LVCMOS | Programmable Alarm 2 set over MDIO, MSA Default: MOD_READY, “1”: Ready, “0”: not Ready |
| 35 | PRG_ALRM3 | O | LVCMOS | Programmable Alarm 3 set over MDIO, MSA Default: MOD_FAULT, fault detected, “1”: Fault, “0”: No Fault |
| 36 | TX_DIS | I | LVCMOS w/PUR | Transmitter Disable for all lanes, “1” or NC=transmitter disabled,”0”=transmitter enabled |
| 37 | MOD_LOPWR | I | LVCMOS w/PUR | Module Low Power Mode.”1” or NC: module in low power(safe) mode, “0”: power-on enabled |
| 38 | MOD_ABS | O | GND | Module Absent “1” or “NC”: module absent, “0”: module present, Pull Up Resistor in Module |
| 39 | MOD_RSTn | I | LVCMOS w/PDR | Module Reset. “0” reset the module, “1” or NC=module enabled, Pull Down Resistor in Module |
| 40 | RX_LOS | O | LVCMOS | Receiver Loss of Optical Signal, “1”: low optical signal, “0”: normal condition |
| 41 | GLB_ALRMn | O | LVCMOS | Global Alarm, “0” :alarm condition in any MDIO Alarm register, “1”: no alarm condition, Open Drain, Pull up Resistor on Host |
| 42 | PRTADR4 | I | 1.2V CMOS | MDIO Physical Port address bit4 |
| 43 | PRTADR3 | I | 1.2V CMOS | MDIO Physical Port address bit3 |
| 44 | PRTADR2 | I | 1.2V CMOS | MDIO Physical Port address bit2 |
| 45 | PRTADR1 | I | 1.2V CMOS | MDIO Physical Port address bit1 |
| 46 | PRTADR0 | I | 1.2V CMOS | MDIO Physical Port address bit0 |
| 47 | MDIO | I/O | 1.2V CMOS | Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba) |
| 48 | MDC | I | 1.2V CMOS | Management Data Clock(Electrical specs as per 802.3ae and ba) |
| 49 | GND | | | |

| | | | | |
|---|---|---|---|---|
| 50 | VND_IO_F | I/O | | Module Vendor I/O F. Do Not Connect |
| 51 | VND_IO_G | I/O | | Module Vendor I/O G. Do Not Connect |
| 52 | GND | | | |
| 53 | VND_IO_H | I/O | | Module Vendor I/O H. Do Not Connect |
| 54 | VND_IO_J | I/O | | Module Vendor I/O J. Do Not Connect |
| 55 | 3.3V_GND | | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal |
| 56 | 3.3V_GND | | | |
| 57 | 3.3V_GND | | | |
| 58 | 3.3V_GND | | | |
| 59 | 3.3V_GND | | | |
| 60 | 3.3V | | | 3.3V Module Supply Votage |
| 61 | 3.3V | | | |
| 62 | 3.3V | | | |
| 63 | 3.3V | | | |
| 64 | 3.3V | | | |
| 65 | 3.3V | | | |
| 66 | 3.3V | | | |
| 67 | 3.3V | | | |
| 68 | 3.3V | | | |
| 69 | 3.3V | | | |
| 70 | 3.3V_GND | | | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal |
| 71 | 3.3V_GND | | | |
| 72 | 3.3V_GND | | | |
| 73 | 3.3V_GND | | | |
| 74 | 3.3V_GND | | | |
| 75 | GND | | | |
| 76 | RX_MCLKp | O | CML | Receiver Monitor Clock (Optional) |
| 77 | RX_MCLKn | O | CML | Receiver Monitor Inverted Clock (Optional) |
| 78 | GND | | | |
| 79 | RX0p | O | CML | Output Data |
| 80 | RX0n | O | CML | Inverted Output Data |
| 81 | GND | | | |
| 82 | RX1p | O | CML | Output Data |
| 83 | RX1n | O | CML | Inverted Output Data |
| 84 | GND | | | |
| 85 | RX2p | O | CML | Output Data |
| 86 | RX2n | O | CML | Inverted Output Data |
| 87 | GND | | | |
| 88 | RX3p | O | CML | Output Data |

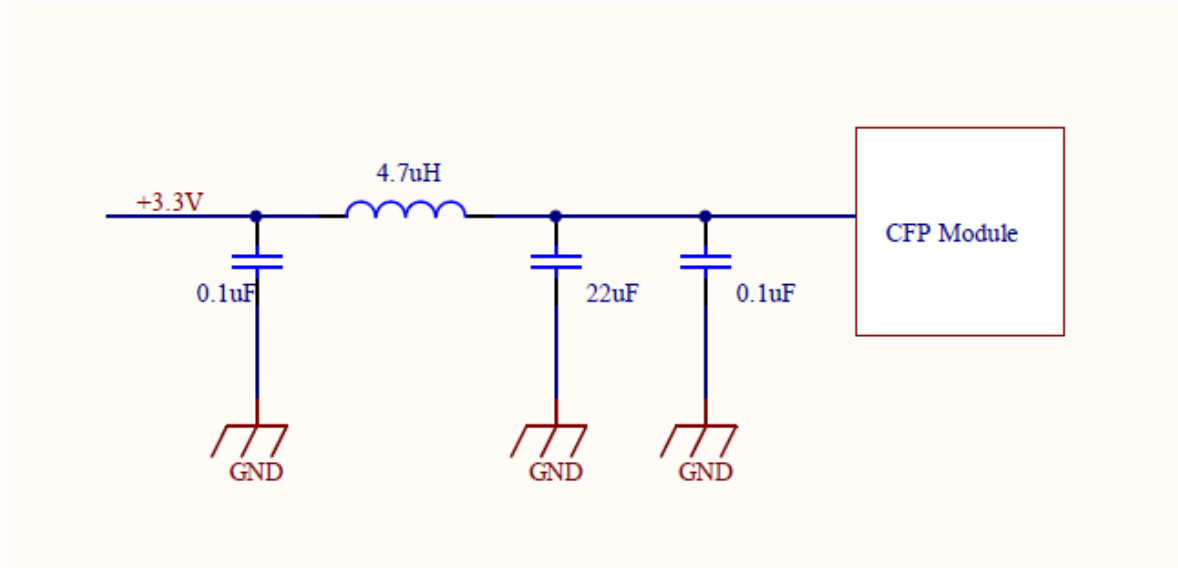
| | | | | |
|---|---|---|---|---|
| 89 | RX3n | O | CML | Inverted Output Data |
| 90 | GND | | | |
| 91 | RX4p | O | CML | Output Data |
| 92 | RX4n | O | CML | Inverted Output Data |
| 93 | GND | | | |
| 94 | RX5p | O | CML | Output Data |
| 95 | RX5n | O | CML | Inverted Output Data |
| 96 | GND | | | |
| 97 | RX6p | O | CML | Output Data |
| 98 | RX6n | O | CML | Inverted Output Data |
| 99 | GND | | | |
| 100 | RX7p | O | CML | Output Data |
| 101 | RX7n | O | CML | Inverted Output Data |
| 102 | GND | | | |
| 103 | RX8p | O | CML | Output Data |
| 104 | RX8n | O | CML | Inverted Output Data |
| 105 | GND | | | |
| 106 | RX9p | O | CML | Output Data |
| 107 | RX9n | O | CML | Inverted Output Data |
| 108 | GND | | | |
| 109 | N.C | | | |
| 110 | N.C | | | |
| 111 | GND | | | |
| 112 | GND | | | |
| 113 | TX0p | In | CML | Input Data |
| 114 | TX0n | In | CML | Inverted Input Data |
| 115 | GND | | | |
| 116 | TX1p | In | CML | Input Data |
| 117 | TX1n | In | CML | Inverted Input Data |
| 118 | GND | | | |
| 119 | TX2p | In | CML | Input Data |
| 120 | TX2n | In | CML | Inverted Input Data |
| 121 | GND | | | |
| 122 | TX3p | In | CML | Input Data |
| 123 | TX3n | In | CML | Inverted Input Data |
| 124 | GND | | | |
| 125 | TX4p | In | CML | Input Data |
| 126 | TX4n | In | CML | Inverted Input Data |
| 127 | GND | | | |
| 128 | TX5p | In | CML | Input Data |
| 129 | TX5n | In | CML | Inverted Input Data |

| | | | | |
|---|---|---|---|---|
| 130 | GND | | | |
| 131 | TX6p | In | CML | Input Data |
| 132 | TX6n | In | CML | Inverted Input Data |
| 133 | GND | | | |
| 134 | TX7p | In | CML | Input Data |
| 135 | TX7n | In | CML | Inverted Input Data |
| 136 | GND | | | |
| 137 | TX8p | In | CML | Input Data |
| 138 | TX8n | In | CML | Inverted Input Data |
| 139 | GND | | | |
| 140 | TX9p | In | CML | Input Data |
| 141 | TX9n | In | CML | Inverted Input Data |
| 142 | GND | | | |
| 143 | N.C. | | | |
| 144 | N.C. | | | |
| 145 | GND | | | |
| 146 | REFCLKp | In | CML | Reference Input Clock |
| 147 | REFCLKn | In | CML | Reference Inverted Input Clock |
| 148 | GND | | | |

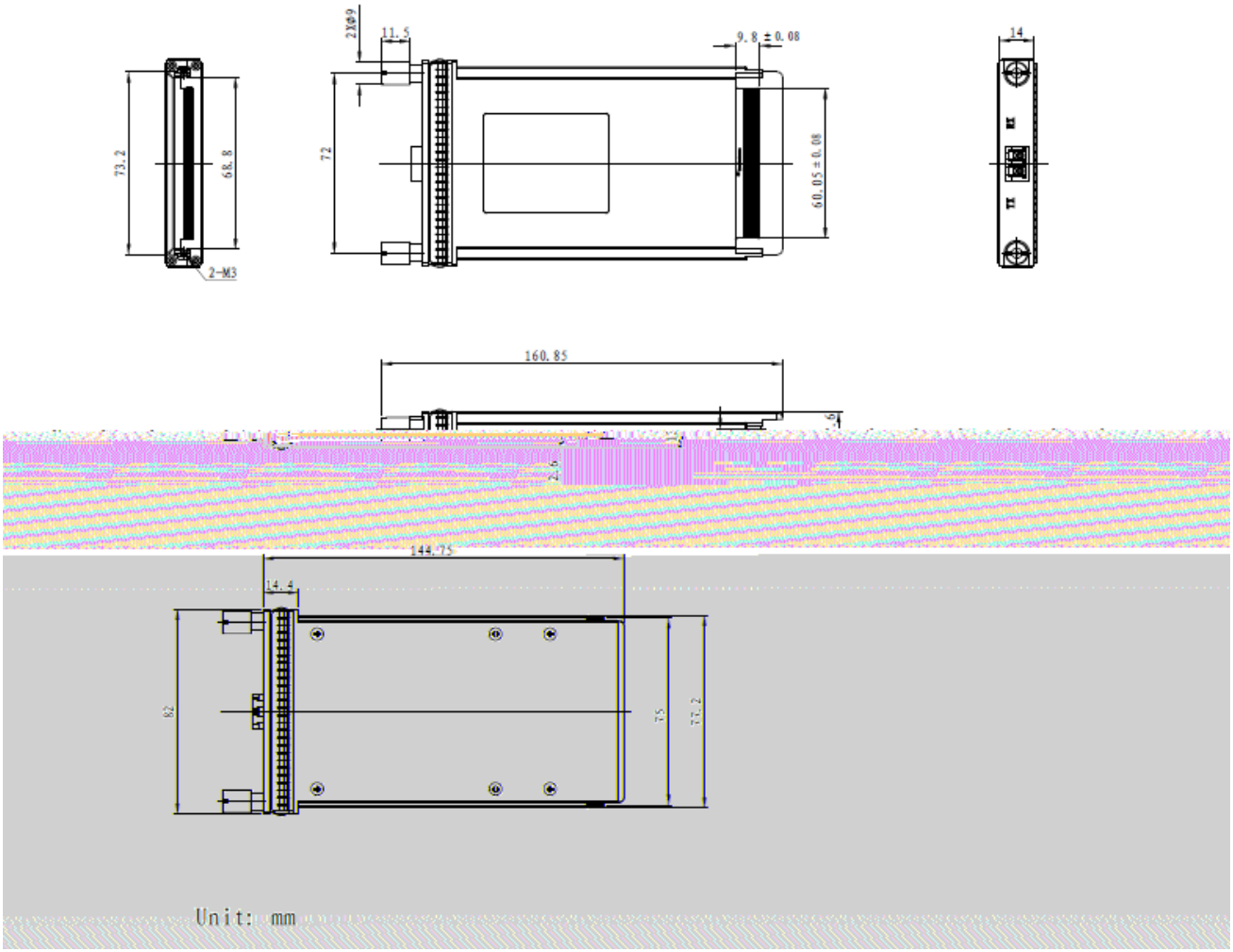
# Block diagram



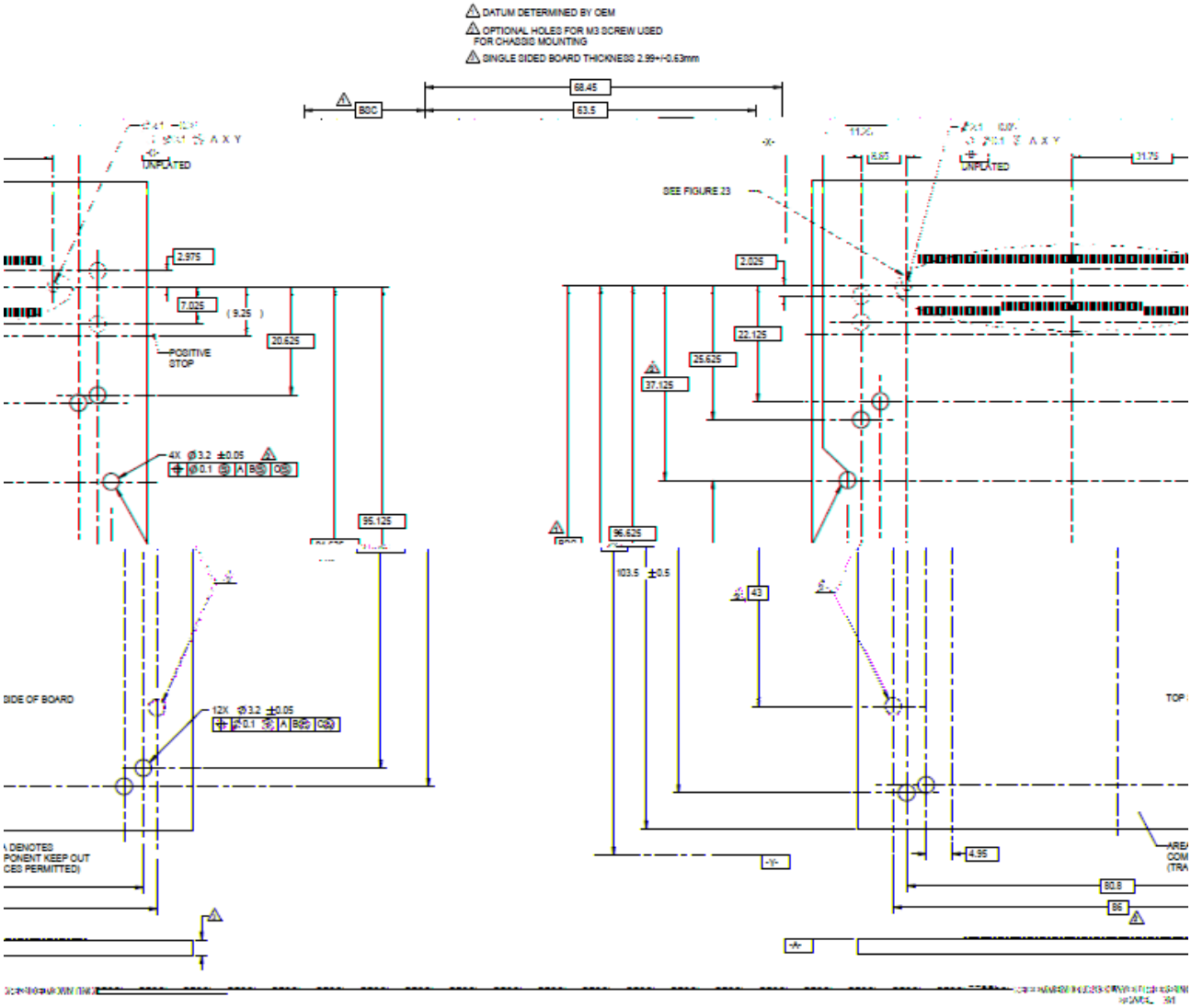

# Required Host Board Components

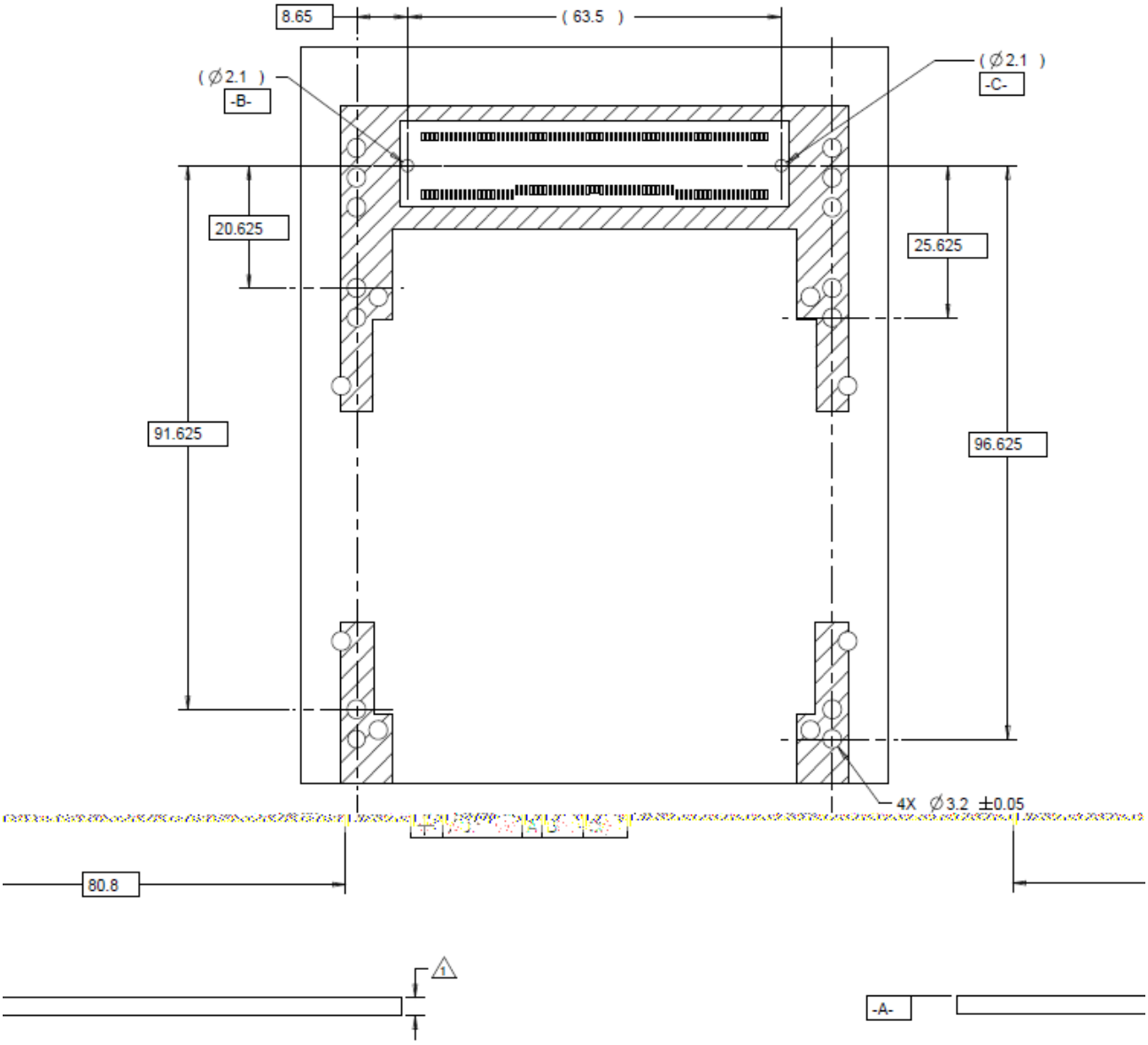


# Package outline




# PCB layout recommendation

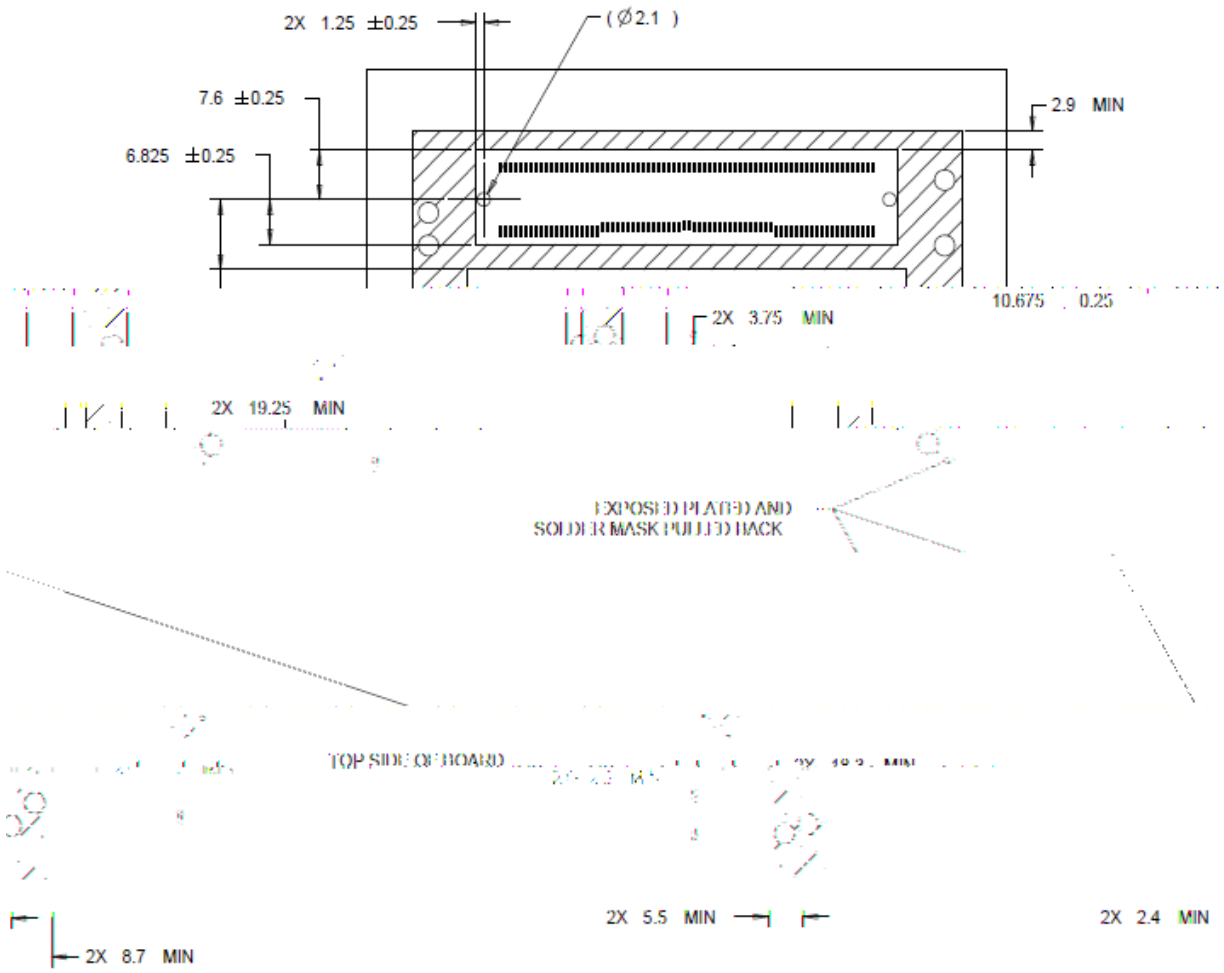

DATUM DETERMINED BY OEM
OPTIONAL HOLES FOR M3 SCREW USED FOR CHASSIS MOUNTING
SINGLE SIDED BOARD THICKNESS 2.99+/-0.63mm
68.45
63.5
BOC
UNPLATED
SEE FIGURE 23
2.975
7.025
( 9.25 )
20.625
POSITIVE STOP
4X Ø3.2 ±0.05
95.125
2.025
22.125
25.625
37.125
96.625
103.5 ±0.5
43
12X Ø3.2 ±0.05
SIDE OF BOARD
TOP
4.95
80.8
86




BOARD THICKNESS 3.40+/-0.40mm

1 BELLY TO BELLY

FIGURE 21




# Regulatory Compliance

| Feature | Test Method | Performance |
|---|---|---|
| Electrostatic Discharge (ESD) to the Electrical Pins | MIL-STD-883E Method 3015.7 | high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B<br>the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B |
| Electrostatic Discharge (ESD) Immunity | IEC61000-4-2 Class B | 15kV air discharges during operation and 8kV direct contact discharge |
| Electromagnetic Interference (EMI) | CISPR22 ITE Class B<br>FCC Class B | Compliant with standard |

| | | |
|---|---|---|
| | CENELEC<br>EN55022<br>VCCI Class 1 | |
| Immunity | IEC61000-4-3<br>Class 2 | Compliant with any electo-magnetic regulations |
| Safety | FDA<br>CDRH 21-CFR 1040 Class 1 | |
| | UL | |
| | TUV-GS | |
| | CE | |

# Ordering Information

| Part No | Specifications | | | | | | | | | Application Code |
|---|---|---|---|---|---|---|---|---|---|---|
| | Pack | Data rate | Tx | Pout | Rx | S | Top | Reach | Others | |
| RTXM290-404 | CFP | 103.125Gbps | 1310nm<br>LAN<br>Cooled<br>EMA<br>DFB-LD | -4.3~+4.5<br>dBm | PIN | <-8.6dBm | 0~70°C | 10km | DDM | 100GbE/OTU4 |